APPLICATIONS OF A STRAIN-COMPENSATED HEAVILY DOPED ETCH STOP FOR SILICON STRUCTURE FORMATION

FIELD OF THE INVENTION

The present invention relates to the formation of a diaphragm in silicon fabrication by etching. More particularly the invention relates to an improved etch stop suitable for use in fabricating a variety of silicon based products such as pressure sensors, accelerometers and other devices using etched diaphragms without adversely affecting the mechanical integrity of the resulting silicon product.

BACKGROUND OF THE INVENTION

The formation of the diaphragm is one of the key steps in silicon pressure sensor fabrication. Likewise, formation of the proof mass and suspension flexures is a key step in the fabrication of a silicon accelerometer. At the present time there are two kinds of electrochemical etches in use for diaphragm etching.

When anisotropic etchants, such as potassium hydroxide or ethylenediamine/pyrocatechol mixtures are used to form diaphragms or flexures, an etch stop is required to prevent the etchant from etching all the way through the silicon wafer. The diaphragm or flexure thickness is determined by this etch step.

One form of etch stop, the electrochemical etch stop, is obtained by applying a positive voltage to n-type portions of the wafer during etching. A p-n junction prevents current from flowing into p-type portions of the wafer, allowing them to etch. However, n-type portions of the wafer are passivated against etching by the applied current. This approach has been used to make pressure sensor diaphragms, and requires electrical contact to the wafer during etching, uniform distribution of current, great care to prevent or minimize leakage current across the p-n junctions, and electrochemical control equipment.

An alternative that is also well known is doping silicon very heavily with boron, greater than $7x10^{19}$ cm^{-3} causes a significant decrease in the etch rate, this being the so-called p+ etch stop. This etch stop effect can be used to form the diaphragm of a pressure sensor, by applying a p+ layer (greater than $7x10^{19}$ cm^{-3}) on a lightly doped substrate (less than about $5x10^{19}$ cm^{-3}) on which electronic

components are fabricated on the surface. These components can be dielectrically isolated piezoresistors or resonant microbeams, as well as temperature compensation and signal conditioning electronics if desired. A mask, using a passivating material such as SiO_2 or SiN_x, is then formed on the back side of the waver, and aligned with the features on the front side. The silicon is then etched by immersion in the etchant, until etching stops at the p+ layer and the wafer is removed from the etchant.

The p+ etch stop can be used in the formation of a dual-web biplane design. This approach imposes additional requirements in that there must be an etch stop on both sides of the wafer, and etching proceeds from both sides of the wafer at once, not just from one side. Electrochemical etching becomes very difficult, and it has been found that undesirable "cusps" are formed on the back side of flexures when using this approach. The p+ etch stop is usable here, with the requirement that there must be a p+ layer on both sides of the wafer.

The p+ etch stop is preferable to an electrochemical etch stop because of its simplicity, high throughput, higher yield and lower cost. No electrical connections to the wafer are required and no in situ monitoring is needed. Preparation of the p-n junction for electrochemical etching requires great care to prevent or minimize leakage, whereas preparation of the p+ material is as simple as a deposition, diffusion or implant step.

In conventional processes, the heavily doped layer is formed by a diffusion process, such as, for example, using a heavy boron diffusion to form the etch stop. Two diffusion steps are done which create the diaphragm surrounded by a thicker p+ region. The thick p+ region is

anodically bonded to a glass wafer. Then everything but the p+ material is dissolved away in an etchant.

While the p+ etch stop has the distinct advantage of ease and simplicity, when compared to the electrochemical etch stop, it also has two distinct disadvantages. First, because the material is heavily doped, a piezoresistor or other electronic device cannot be formed in it. Second, because the boron atom is smaller than the silicon atom, the heavy concentration of boron causes a contraction of the silicon lattice. This strain generates large numbers of dislocations in the material, making it mechanically poor.

One prior art solution to the electrical problem is to use a p+ "buried layer." In this approach, the p+ etch stop layer is formed, for example, by diffusion or epitaxial growth., followed by a layer of lightly doped material of either n-type or p-type. Electronics, such as piezoresistors, transistors and circuits for compensation, signal processing and communication, can be formed in the lightly doped, low defect density top layer. During diaphragm formation, etching stops on the buried layer, which is then removed by another etchant, such as those known to selectively etch p+ silicon and stops on lightly doped silicon. While this solves the problem of the electronics, the lightly doped layer is still filled with dislocations that propagate from the p+ layer.

It would be of great advantage in the art if a method could be provided for application of strain relieved material to pressure sensors and accelerometers in designs that use the p+ etch stop with highly strained material.

It would be another great advance in the art if difficulties in forming electronics in conjunction with heavily doped material could be provided.

Another advantage would be if appropriately strain compensated layers as thin as a thousand Ångstroms or as thick as several tens of microns could be achieved.

Other advantages will appear hereinafter.

SUMMARY OF THE INVENTION

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, the present invention comprises the use of a strain compensated material that can be used to form pressure sensor diaphragms, cantilevered accelerometers, dual-web biplane accelerometer structures and resonant microbeam formation.

The present invention comprises a method of making a silicon micromechanical structure. The method, and the devices produced thereby, include the use of a large atom, germanium, which is codoped with the boron, giving the silicon substrate a balance of small boron atoms and larger germanium atoms, forming a strain relieved etch stop layer. Germanium is isoelectronic with silicon. Strain compensated layers as thin as one thousand Ångstroms and as thick as several tens of microns are contemplated.

Lightly doped silicon, which is used as the substrate in this invention, is defined as silicon wafers having includes less than $5x10^{19}$ cm^{-3} boron therein. A p+ or highly doped layer is put on one side of a lightly doped silicon substrate. Highly doped silicon, or a p+ layer, is defined as having a boron content of greater than $7x10^{19}$ cm^{-3} and also a germanium content of about $1x10^{21}$ cm^{-3}. Preferred are p+ layers where the boron content is greater than $1x10^{20}$ cm^{-3} and the germanium content is from about 0.5 $x10^{21}$ cm^{-3} to about 2.0 $x10^{21}$ cm^{-3}.

In another embodiment, the method of this invention, and the devices formed thereby, includes the use of a lightly doped layer on top of the p+ layer, burying the p+ layer and used in the same manner. In this embodiment, it is optionally possible to etch the buried p+ layer as part of the formation of the devices of the present invention.

Once the p+ layer has been applied, a mask is formed on the back or bottom side of the wafer for etching a predetermined pattern. The back side is then etched in a conventional manner to the p+ layer. An insulator is deposited on the p+ layer, after which an electronic component on said insulator is fabricated, again using conventional semiconductor techniques, to form a micromechanical structure. Preferred micromechanical structures are pressure sensors, cantilevered accelerometers, and dual web biplane accelerometer. Preferred electronic component are dielectrically isolated piezoresistors and resonant microbeams.

In another embodiment, the micromechanical structure includes a dielectrically isolated piezoresistor formed on a top surface of a first wafer, a second wafer is bonded to said first wafer, and said second wafer forms a single crystal piezoresistor.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the invention, reference is hereby made to the drawings, in which:

FIGS. 1a, 1b, 1c, and 1d are schematic views in section of a wafer employing a first embodiment of the present invention, used to form a pressure sensor;

FIGS. 2a, 2b, 2c, and 2d are schematic views in section of a wafer employing this first embodiment of the present invention, used to form a cantilevered accelerometer;

FIGS. 3a, 3b, 3c, 3d, 3e, 3f, and 3g are schematic views of in section of a wafer employing this first embodiment of the present invention used, to form a dual web biplane accelerometer;

FIGS. 4a, 4b, 4c, 4d and 4e are schematic views in section of a wafer employing the second embodiment of the present invention, used to form a pressure sensor;

FIGS. 5a, 5b, 5c, 5d and 5e are schematic views in section of a wafer employing the second embodiment of the present invention, used to form a cantilevered accelerometer; and

FIGS. 6a, 6b, 6c, 6d, 6e, 6f, 6g and 6h are schematic views in section of a wafer employing this second embodiment of the present invention, used to form a dual web biplane accelerometer;

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention has been used to form a number of microstructures on silicon wafers, shown in all the figures as wafer 11 having a first side 13 and a second side 15.

Shown in Figs. 1a-1d is the formation of a pressure sensor. In Fig. 1a, a lightly doped wafer 11 has p+ layer 17 formed on side 13, wherein layer 17 is with boron and germanium to form highly doped silicon. Lightly doped silicon is defined as silicon wafers having includes less than $5x10^{19}$ cm^{-3} boron therein. Highly doped silicon, or a p+ layer, is defined as having a boron content of greater than $7x10^{19}$ cm^{-3} and also a germanium content of about $1x10^{21}$ cm^{-3}. Preferred are p+ layers where the boron content is greater than $1x10^{20}$ cm^{-3} and the germanium ranges from about $0.5\ x10^{21}$ cm^{-3} to about $2.0\ x10^{21}$ cm^{-3}.

Electronics 19 are fabricated on the p+ layer 17 in a conventional manner, and can be dielectrically isolated piezoresistors or resonant microbeams. A mask 21 for diaphragm masking is formed on second side 15, normally aligned with the electronics 19 on first side 13. Etching takes place, as seen in Fig. 1d, until it reaches the p+ layer 17. Because of the presence of germanium in the boron doped p+ layer 17, strain in the silicon has been compensated and the device operates in an improved, longer lasting manner.

Figs. 2a-2d illustrate the formation of a cantilevered accelerometer in accordance with one preferred embodiment of the

present invention. A p+ layer 17 is formed on side 13 of lightly doped wafer 11. Electronics 19 are again fabricated on the p+ layer 17 in a conventional manner, and can be dielectrically isolated piezoresistors or resonant microbeams. A mask 21 for proof mass and flexure etching is formed on second side 15, normally aligned with the electronics 19 on first side 13. Etching takes place, as seen in Fig. 2d, until it reaches the p+ layer 17. Again, because of the presence of germanium in the boron doped p+ layer 17, strain in the silicon has been compensated and the devices operate in an improved, longer lasting manner.

Figs. 3a-3g illustrate the formation of a dual web biplane accelerometer using the p+ etch stop concept as described herein. In this embodiment, a first p+ layer 17 is epitaxially grown on side 13 of lightly doped wafer 11 and a second p+ layer 18 is epitaxially grown on the other side 15 of wafer 11. Electronics 19 are once again fabricated on the p+ layer 17 in a conventional manner, and additional electronics 20 are fabricated on p+ layer 18. It is intended that a wide variety of electronics may be used. Here, a piezoelectric resistor may be formed in the lightly doped layer 11, or dielectrically isolated piezoresistors or resonant microbeams. Mask 21 and 22 for proof mass and flexure etching are formed on both sides 13 and 15 respectively, with the masks 21 and 22 aligned with the electronics 19 and 20. Etching into the silicon wafer 11 takes place, as seen in Figs. 3c through 3g, until it reaches the p+ layer 17, producing an improved dual web biplane accelerometer because of the boron and germanium doping to produce an etch stop with the p+ layer.

In Figs. 4a-4e, another pressure sensor is formed, using a second embodiment of the present invention where p+ layer 17 is covered by an epitaxially grown lightly doped layer 23, formed on side 13, wherein layer 17 is with boron and germanium to form highly doped silicon. As in Figs. 1a-1d, electronics 19 are fabricated on the p+ layer 17, a mask 21 for diaphragm masking is formed on second side 15, normally aligned with the electronics 19 on first side 13. Etching takes place, as seen in Fig. 1d, until it reaches the p+ layer 17. In Fig. 4e, an optional step is shown where p+ layer is also removed by etching, using a commercially available p+ selective etchant.

The cantilevered accelerometer shown in Figs. 5a-5e is similar to that shown if Figs. 2a-2d, again using a lightly doped, epitaxially grown cover layer 23 for the p+ layer 17. Etching of the silicon is stopped at p+ layer, as before, and again optional removal of the p+ layer is shown in Fig. 5e.

The dual web biplane accelerometer shown in Figs. 6a-6h is similar to that shown in Figs. 3a-3g, again using a lightly doped, epitaxially grown cover layer 23 for both the p+ layer 17 and a second p+ layer 18. Electronics 19 and 20 are fabricated on the lightly doped layers 23 p+ layers 17 and 18 respectively. Mask 21 and 22 for proof mass and flexure etching are formed on both sides 13 and 15 respectively, with the masks 21 and 22 aligned with the electronics 19 and 20. Etching into the silicon wafer 11 takes place, as seen in Figs. 6c through 6g, until it reaches the p+ layer 17, producing an improved dual web biplane accelerometer because of the boron and

germanium doping to produce an etch stop with the p+ layer. Optional removal of the p+ layer is shown in Fig. 6h.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.